IN THE ABSTRACT

~~An integrated circuit chip is provided having a plurality of embedded RAM/register blocks, a corresponding plurality of test modules,~~ and a ~~dedicated test bus. Each RAM/register block is coupled to a corresponding test module, as well as to system circuitry. Each test module is coupled to the test bus. The embedded RAM/register blocks are accessible through the system circuitry during normal operation. During a test mode the embedded RAM/register blocks are accessible through the test modules and test bus. During the test mode, test data values are written to the RAM/register blocks by broadcasting test data values to all of the RAM/register blocks on the test bus. Subsequently, the test data values are read from the RAM/register blocks by individually accessing the RAM/register blocks on the test bus. The test modules are assigned unique addresses, thereby enabling the RAM/register blocks to be addressed during the read operations.~~

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A test bus architecture for an integrated circuit chip including a plurality of embedded RAM/register blocks, a corresponding plurality of test modules, and a dedicated test bus. Each RAM/register block is coupled to a corresponding test module, as well as to system circuitry. Each test module is coupled to the test bus. The embedded RAM/register blocks are accessible through the system circuitry during normal operation. During a test mode the embedded RAM/register blocks are accessible through the test modules and test bus. During the test mode, test data values are written to the RAM/register blocks by broadcasting test data values to all of the RAM/register blocks on the test bus. Subsequently, the test data values are read from the RAM/register blocks by individually

accessing the RAM/register blocks on the test bus. The test modules are assigned unique addresses, thereby enabling the RAM/register blocks to be addressed during the read operations.